OpSIS Public Run #1:
IME Silicon Photonics Process

Silicon photonics process in a state of the art fabrication facility

OpSIS (http://depts.washington.edu/uwopsis/) is offering a multi-project wafer run in IME's silicon photonics process for tapeout in the fall of 2011.

IME's silicon photonics process is run in a standard microelectronics facility and offers a basic set of optical devices to build upon. The overview of the process offered is shown in Table 1. This process is as simple as possible while still delivering high performance optical devices and the convenience of grating couplers for wafer-level testing, as well as the ability to edge coupler if needed.

IME Process at a glance	
Parameter/Device Type	**Features**
Overview	• 220 nm thick starting Si, 2um BOX • High resistivity handle (750 ohm.cm) • Photonics-only process, no electronics included
Front-end	• Two partial etches, 1 full etch of top silicon • 6 optical implants for modulators • 100% Ge deposition and implanting
Back-end	• Two metal levels, no planarization • Deep Si Trench for edge coupling
Optical library devices	• Grating couplers • Low loss waveguides (ridge and rib) • High-speed MZI modulators (reverse-biased pn junction) • High-speed Ge waveguide photodiodes

Table 1: IME provess overview

The rest of this document provides a detailed overview of the offering:

- Process cross-section example
- Typical and minimal guaranteed performance for optical devices
- Critical process-related performance parameters
- Test results from qualification silicon

- Schedule
- Cost
- Administrative formalities required to participate in the run

<u>Important note:</u> this is a preliminary document and the values and ranges provided are for information only. Exact specifications will be provided at a later date. Prospective users are encouraged to contact OpSIS to obtain more information.

Process cross-section schematic

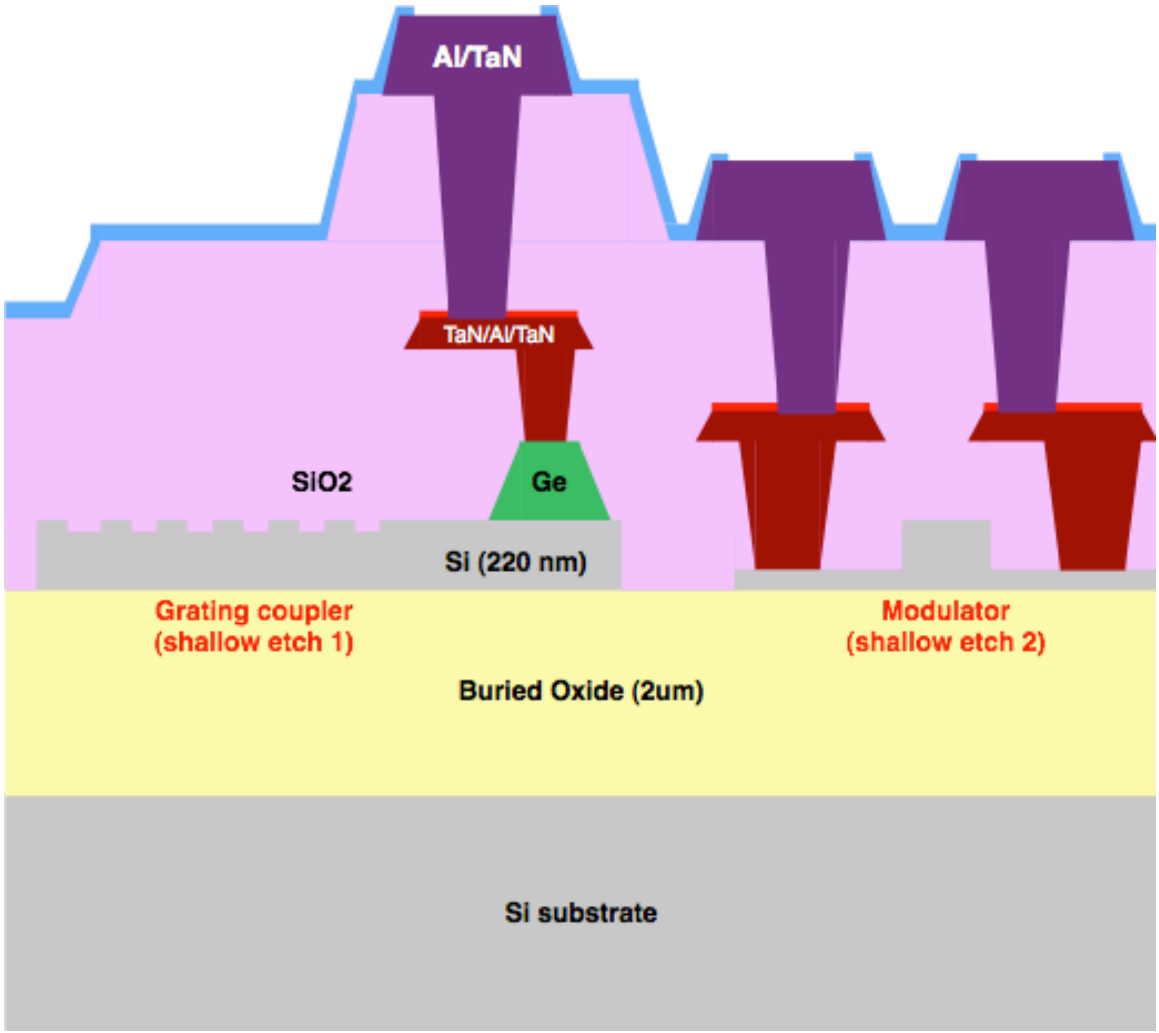

Figure 1: Process cross-section

Optical performance parameters

The parameters in Table 2 will be guaranteed for the unit cells provided by OpSIS and IME. Any variations on the layout or design of these unit cells will not be guaranteed.

Optical performance parameters overview				
Device	**Typical performance**	**Typ**	**Min/Max**	**Units**
Edge Coupler	Insertion loss/facet	3	4.5	dB
Waveguide (single mode)	Propagation loss	3	4	dB/cm
High-speed Mach-Zehnder modulator	Phase shifter length	4	N.A.	mm
	Insertion loss	7	8	dB
	Extinction ratio (5 Gb/s, Vpp = 6V, Vdc = -3.5V)	8	5	dB
Ge photodiode	Waveguide length	100	N.A.	um
	Bandwidth (-1V, 50 ohms)	5	5	GHz
	Dark current (-1V)	0.5	1	uA
	Responsivity (1550 nm)	0.8	0.5	A/W

Table 2: Optical performance parameters table

Critical process parameters

Process parameters overview			
Parameter	**Target**	**Range (+/-)**	**Units**
SOI thickness	220	20	nm
Handle resistivity	> 750		ohm.cm
Si partial etch 1 (depth)	60	15	nm
Si partial etch 2 (depth)	130	25	nm
Ge epi thickness	500		nm
ILD0 thickness (contact dielectric)	600	60	nm
Metal 1 (Al) thickness	750		nm
Contact resistivity (Metal 1 to Si)	< 5e-6		ohms.cm^2
Contact resistivity (Metal 1 to Ge)	< 5e-6		ohms.cm^2
Metal 1 sheet resistance	< 100		mohms/sq
ILD1 thickness (via dielectric)	1500	150	nm
Metal 2 (Al) thickness	2000		nm
Metal2 sheet resistance	35		mohms/sq

Table 3: Critical process parameters

Test results from silicon qualification run

All results were obtained using wafer-scale testing with grating couplers as optical I/Os.

Passive optical performance results

Contour maps of grating coupler peak insertion loss and waveguide loss are shown in Figure 2, along with a typical grating coupler spectrum. The average grating coupler peak insertion loss was 4.37 dB. Waveguide loss for 500 nm channel waveguides was 2.35 dB/cm on average.

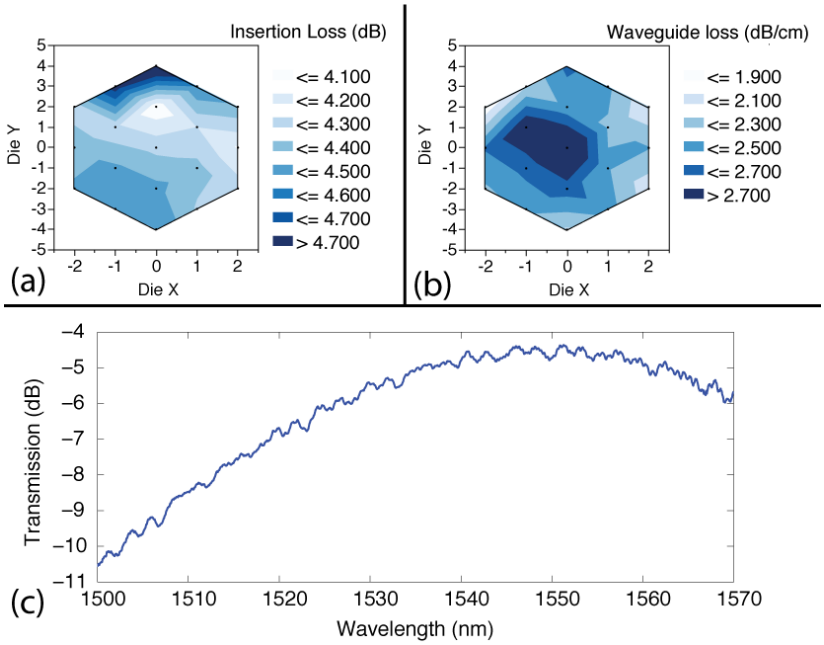

Figure 2: wafer-scale contour maps for (a) grating coupler peak insertion loss and (b) waveguide loss, along with (c) a typical grating coupler insertion loss spectrum

Germanium photodetector performance

15 um devices were tested, providing a good tradeoff between responsivity at 1550 nm and bandwidth.

Wafer-scale plots for responsivity, dark current, and 3dB bandwidth at 1V and 4V reverse bias are shown in Figure 3. Figure 4 shows typical frequency response curves at 1 and 4 V bias.

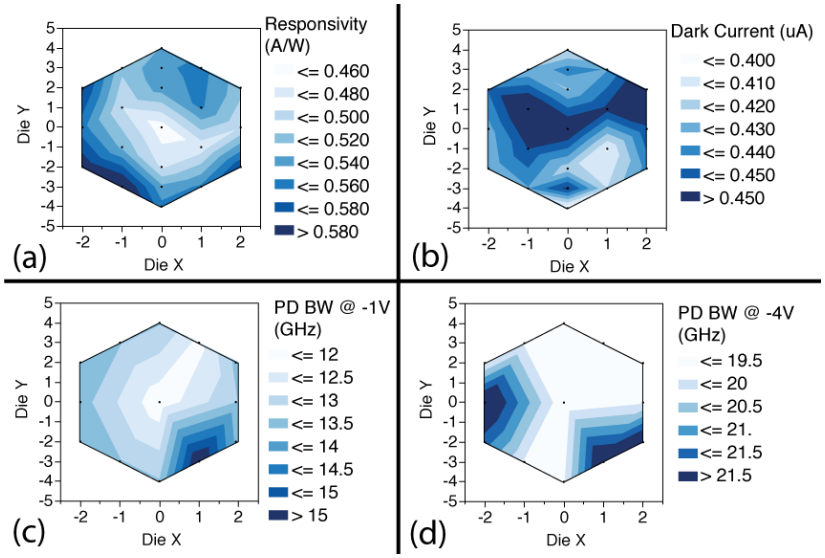

Figure 3: wafer-scale contour plots of (a) responsivity at 1550 nm, (b) dark current at 1V bias, (c) bandwidth at 1 V bias, and (d) bandwidth at 4V bias

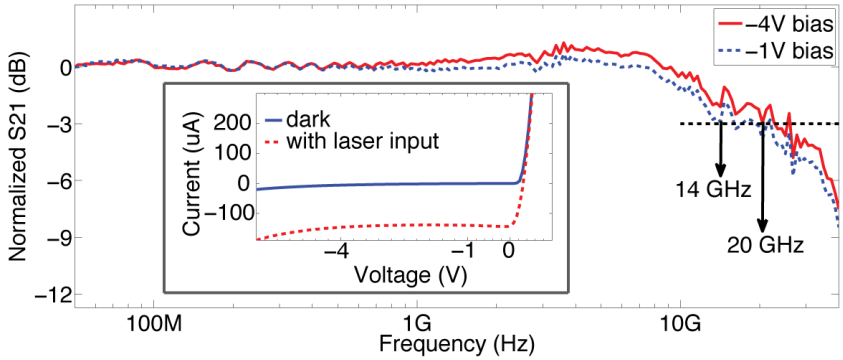

Figure 4: Typical frequency response curves of a Ge photodiode at 1 and 4 V bias

Modulator performance

Ring and traveling-wave MZI modulators were tested. Performance is summarized in Figure 5, Figure 6, and Figure 7.

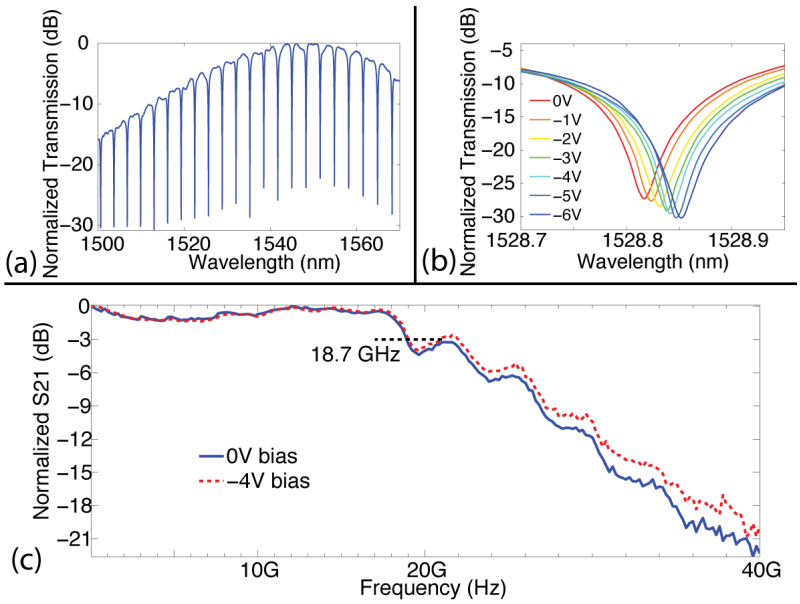

Figure 5: (a) typical ring spectrum, (b) Tunability curves, and (c) frequency response at 0 and 4V bias

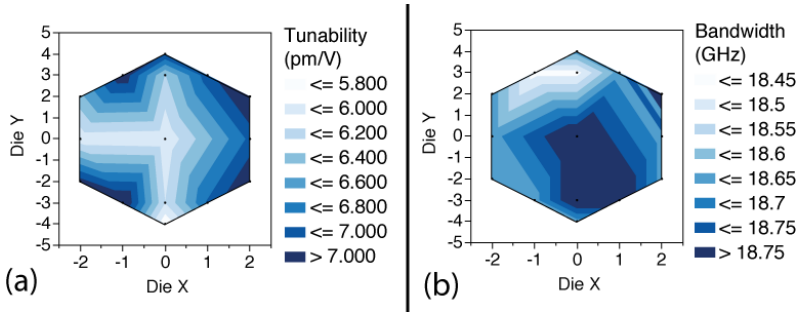

Figure 6: Wafer-scale contour maps of (a) DC tunabillity and (b) bandwidth

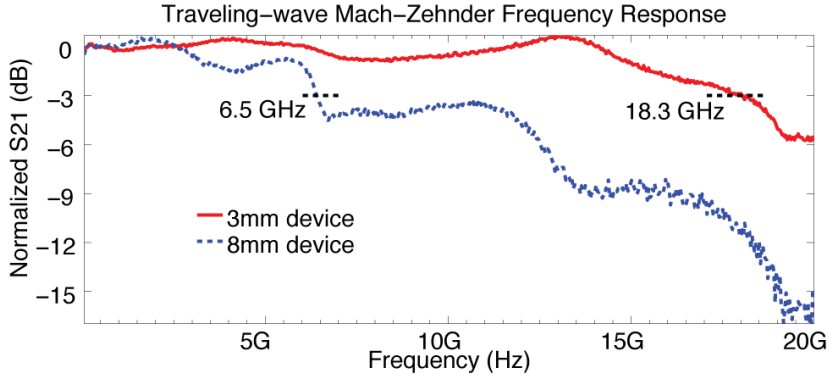

Figure 7: Typical frequency response curves of traveling wave modulators of 3 and 8 mm length

Schedule

The following milestones are projected for the first public run with OpSIS/IME:

Date	Milestone
11/15/2011	Deadline for sign-up with OpSIS for participation in the run
11/30/2011	initial floorplan; requires users to have finalized their design area and aspect ratio
12/15/2011	Design Rule waivers request submitted to OpSIS
01/16/2011	Final DRC clean/waivered GDS submitted to OpSIS
05/30/2012	Delivery of chips to users

Table 4: Tentative milestones for OpSIS/IME public run #1

Cost

Participation in the run will be billed on an area basis, as explained in the table below:

Item	
Cost ($/mm^2 of chip area)	1500.00
Minimum required subscription (mm^2)	10
Deliverables (number of diced parts)	>= 20
Minimum total subscribed area required (mm^2)	250*

* run may not happen if we do not manage to obtain the minimum required area

Table 5: Cost for participation in the run

Note that we are currently evaluating avenues for offering users the option to purchase full wafers (with other users' IP/designs destroyed), but we cannot guarantee this will be available on the first run.

Requirements for participation

To be able to participate in the run, your institution will be required to:

- Sign the 3-way NDA with OpSIS and IME and pass our restricted persons list check for export control compliance
- Sign the user agreement
- Fill out questionnaires, notably on export control compliance that allow OpSIS to determine proper export control classification
- Fill out a project order form to subscribe are on the run

All the relevant forms will be available online at
http://depts.washington.edu/uwopsis/